THAT WHICH IS CLAIMED IS:

1. A capacitor having a dielectric structure comprising:

a silicon carbide layer

a first oxide layer having a first thickness on the silicon carbide layer;

a layer of dielectric material on the first oxide layer and having a second thickness, the layer of dielectric material having a dielectric constant higher than the dielectric constant of the first oxide layer;

a second oxide layer on the layer of dielectric material opposite the first oxide layer and having a third thickness; and

wherein the first thickness is between about 0.5 and about 33 percent and the second thickness is between about 0.5 and about 33 percent of the sum of the first, second and third thicknesses.

2. The capacitor of Claim 1, further comprising:

a first metal layer on the first oxide layer opposite the layer of dielectric material and disposed between the first oxide layer and the silicon carbide layer; and

a second metal layer on the second oxide layer opposite the high dielectric layer so as to provide a metal-insulator-metal (MIM) capacitor.

3. The capacitor of Claim 2, wherein the first oxide layer and the second oxide layer comprise silicon dioxide and wherein the layer of dielectric material comprises at least one of silicon nitride and silicon oxynitride.

4. The capacitor of Claim 3, wherein the first thickness and the third thickness are at least about one order of magnitude smaller than the second thickness.

5. The capacitor of Claim 3, wherein the first thickness is from about 10 to about 30 nm, the second thickness is from about 200 to about 300 nm and the third thickness is from about 10 to about 30 nm.

6. The capacitor of Claim 3, wherein at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured so that the dielectric structure has a mean time to failure versus voltage characteristic which has a greater slope than a corresponding MIM capacitor with only a nitride dielectric.

7. The capacitor of Claim 3, wherein the silicon dioxide layers and the silicon nitride layer are deposited layers.

8. The capacitor of Claim 2, wherein at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured to provide a mean time to failure of at least about 10^7 hours at a voltage of greater than about 50 volts and a temperature of at least about 100 °C.

9. The capacitor of Claim 8, wherein at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured to provide a mean time failure of at least about 10^7 hours at a voltage of greater than about 100 volts and a temperature of at least about 100 °C.

10. The capacitor of Claim 2, wherein the first and second metal layers comprise at least one of titanium, platinum, chromium and gold.

11. The capacitor of Claim 2, further comprising a silicon carbide substrate on which the capacitor is formed.

12. The capacitor of Claim 11, further comprising a plurality of semiconductor devices formed in the silicon carbide substrate.

13. A high mean time to failure interconnection structure for an integrated circuit, comprising:

a plurality of semiconductor devices in a SiC substrate;

an insulating layer on the plurality of semiconductor devices;

a first interconnect layer having a plurality of regions of interconnection metal on the insulating layer opposite the plurality of semiconductor devices;

a first layer of oxide on the first interconnect layer so as to cover at least a portion of the plurality of regions of interconnection metal;

a layer of dielectric material on the first layer of oxide opposite the first interconnect layer and having a dielectric constant higher than a dielectric constant of the first oxide layer;

a second layer of oxide on the layer of dielectric material opposite the first layer of oxide; and

a second interconnect layer on the second layer of oxide opposite the layer of dielectric material and having a plurality of regions of interconnection metal.

14. The interconnection structure of Claim 13, wherein the first oxide layer and the second oxide layer comprise silicon dioxide layer and wherein the layer of dielectric material comprises silicon nitride.

15. The interconnection structure of Claim 14, wherein the first oxide layer has a thickness of from about 10 to about 30 nm, the layer of dielectric material has a thickness of from about 200 to about 300 nm and the second oxide layer has a thickness of from about 10 to about 30 nm.

16. The interconnection structure of Claim 13, wherein the first oxide layer has a first thickness, the layer of dielectric material has a second thickness and the second oxide layer has a third thickness and wherein the first thickness and the third thickness are at least about one order of magnitude smaller than the second thickness.

17. The interconnection structure of Claim 16, wherein at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured to provide a mean time to failure versus voltage characteristic which has a greater slope than a corresponding nitride inter-metal dielectric.

18. The interconnection structure of Claim 14, wherein the silicon dioxide layers and the silicon nitride layer are deposited layers.

19. The interconnection structure of Claim 13, wherein at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured to provide a mean time to failure of at least about 10^7 hours at a voltage of greater than about 50 volts and a temperature of at least about 100 °C.

20. The interconnection structure of Claim 19, wherein at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are

configured to provide a mean time failure of at least about 10^7 hours at a voltage of greater than about 100 volts and a temperature of 150 °C.

21. The interconnection structure of Claim 13, wherein the interconnect metal of the first and second interconnect layers comprise at least one of titanium, platinum, chromium and gold.

22. A method of fabricating a capacitor, comprising:

depositing a first oxide layer on a first metal layer so as to provide a first oxide layer having a first thickness;

depositing a layer of dielectric material on the first oxide layer to provide a high dielectric layer having a second thickness, the layer of dielectric material having a dielectric constant higher than the dielectric constant of the first oxide layer;

depositing a second oxide layer on the layer of dielectric material opposite the first oxide layer to provide a second oxide layer having a third thickness;

forming a second metal layer on the second oxide layer; and

wherein the first thickness is between about 0.5 and about 33 percent and the second thickness is between about 0.5 and about 33 percent of the sum of the first, second and third thicknesses.

23. The method of Claim 22, wherein the first oxide layer and the second oxide layer comprise silicon dioxide layers and wherein the nitride layer comprises a silicon nitride layer.

24. The method of Claim 22, wherein the first thickness and the third thickness are at least about one order of magnitude smaller than the second thickness.

25. The method of Claim 22, wherein the first thickness is from about 10 to about 30 nm, the second thickness is from about 200 to about 300 nm and the third thickness is from about 10 to about 30 nm.

26. The method of Claim 22, wherein the first and second metal layers comprise at least one of titanium, platinum, chromium and gold.

27. A method of fabricating an interconnection structure for an integrated circuit, comprising:

forming a plurality of semiconductor devices in a substrate;

forming an insulating layer on the plurality of semiconductor devices;

forming a first interconnect layer having a plurality of regions of interconnection metal on the insulating layer opposite the plurality of semiconductor devices;

depositing a first layer of oxide on the first interconnect layer so as to cover at least a portion of the plurality of regions of interconnection metal;

depositing a high dielectric layer on the first layer of oxide opposite the first interconnect layer;

depositing a second layer of oxide on the high dielectric layer opposite the first layer of oxide;

forming a second interconnect layer on the second layer of oxide opposite the high dielectric layer and having a plurality of regions of interconnection metal; and

wherein the first layer of oxide, the high dielectric layer and the second layer of oxide are disposed between corresponding ones of the plurality of regions of interconnection metal of the first interconnect layer and the plurality of regions of interconnection metal of the second interconnect layer so as to provide an inter-metal dielectric structure.

28. The method of Claim 27, wherein the first oxide layer and the second oxide layer comprise silicon dioxide layers and wherein the nitride layer comprises a silicon nitride layer.

29. The method of Claim 28, wherein the first oxide layer has a thickness of from about 10 to about 30 nm, the high dielectric layer has a thickness of from about 200 to about 300 nm and the second oxide layer has a thickness of from about 10 to about 30 nm.

30. The method of Claim 27, wherein the first oxide layer has a first thickness, the high dielectric layer has a second thickness and the second oxide layer has a third thickness and wherein the first thickness and the third thickness are at least about one order of magnitude smaller than the second thickness.

31. The method of Claim 27, wherein the interconnect metal of the first and second interconnect layers comprises at least one of titanium, platinum, chromium and gold.

32. A capacitor comprising:

a silicon carbide layer

a layer of dielectric material on the silicon carbide layer, the layer of dielectric material comprising silicon oxynitride having a formula $Si_3N_{4-X}O_X$, where $0<X\leq 1$;

a first metal layer on the layer of dielectric material opposite the silicon carbide layer.

33. The capacitor of Claim 32, further comprising a second metal layer on the layer of dielectric material and disposed between the layer of dielectric material and the silicon carbide layer so as to provide a metal-insulator-metal (MIM) capacitor.

34. The capacitor of Claim 33, wherein the layer of dielectric material is configured so that the dielectric structure has a mean time to failure versus voltage characteristic which has a greater slope than a corresponding MIM capacitor with only a nitride dielectric.

35. The capacitor of Claim 33, wherein the silicon oxynitride of the layer of dielectric material is a deposited layer.

36. The capacitor of Claim 33, wherein the layer of dielectric material is configured to provide a mean time to failure of at least about 10^7 hours at a voltage of greater than about 50 volts and a temperature of at least about 100 °C.

37. The capacitor of Claim 36, wherein the layer of dielectric material is configured to provide a mean time failure of at least about 10^7 hours at a voltage of greater than about 100 volts and a temperature of at least about 100 °C.

38. The capacitor of Claim 33, wherein the first and second metal layers comprise at least one of titanium, platinum, chromium and gold.

28 22
39. The capacitor of Claim ~~33~~, further comprising a plurality of semiconductor devices formed in the silicon carbide layer.

29
40. A high mean time to failure interconnection structure for an integrated circuit, comprising:

a plurality of semiconductor devices in a silicon carbide substrate;

an insulating layer on the plurality of semiconductor devices;

a first interconnect layer having a plurality of regions of interconnection metal on the insulating layer opposite the plurality of semiconductor devices;

a layer of dielectric material on the first layer of oxide opposite the first interconnect layer, the layer of dielectric material comprising silicon oxynitride having a formula $Si_3N_{4-X}O_X$, where $0<X\leq 1$;

a second interconnect layer on the layer of dielectric material opposite the first interconnect layer and having a plurality of regions of interconnection metal.

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41. The interconnection structure of Claim ~~40~~, wherein the layer of dielectric material has a thickness of from about 20 nm to about 400 nm.

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42. The interconnection structure of Claim ~~40~~, wherein the layer of dielectric material is configured to provide a mean time to failure versus voltage characteristic which has a greater slope than a corresponding nitride inter-metal dielectric.

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43. The interconnection structure of Claim ~~40~~, wherein the layer of dielectric material is a deposited layer of silicon oxynitride.

33 32
44. The interconnection structure of Claim ~~43~~, wherein the layer of dielectric material is configured to provide a mean time to failure of at least about 10^7 hours at a voltage of greater than about 50 volts and a temperature of at least about 100 °C.

34 ~~45.~~ The interconnection structure of Claim 33 ~~44~~, wherein the layer of dielectric material is configured to provide a mean time failure of at least about 10^7 hours at a voltage of greater than about 100 volts and a temperature of 150 °C.

35 ~~46.~~ The interconnection structure of Claim 29 ~~40~~, wherein the interconnect metal of the first and second interconnect layers comprise at least one of titanium, platinum, chromium and gold.

~~47.~~ A method of fabricating a capacitor, comprising:

depositing a layer of silicon oxynitride having a formula $Si_3N_{4-X}O_X$, where $0<X\leq1$, on a silicon carbide layer so as to provide a layer of dielectric material having a first thickness; and

forming a first metal layer on the layer of silicon oxynitride.

48. The method of Claim 47, further comprising forming a second metal layer disposed between the layer of silicon oxynitride and the silicon carbide layer.

49. The method of Claim 47, wherein the first thickness is from about 20 nm to about 400 nm.

50. The method of Claim 48, wherein the first and second metal layers comprise at least one of titanium, platinum, chromium and gold.

51. The method of Claim 47, wherein depositing a silicon oxynitride layer having a formula $Si_3N_{4-X}O_X$, where $0<X\leq1$ comprises:

providing a silicon precursor;

providing a nitrogen precursor;

providing an oxygen precursor; and

depositing the layer of silicon oxynitride utilizing the silicon precursor, the nitrogen precursor and the oxygen precursor utilizing a plasma enhanced chemical vapor deposition (PECVD) process.

52. The method of Claim 51, wherein the silicon precursor comprises SiH_4, the oxygen precursor comprises N_2O and the nitrogen precursor comprises N_2.

53. The method of Claim 52, wherein the SiH_4 is provided at a flow rate of from about 240 to about 360 standard cubic centimeters per minute (SCCM), the N_2O is provided at a flow rate of from about 8 to about 12 SCCM and the N_2 is provided at a flow rate of from about 120 to about 180 SCCM for a PECVD apparatus having a volume of about 14785 cubic centimeters.

54. The method of Claim 53, further comprising providing an inert gas.

55. The method of Claim 54, wherein the inert gas comprises He provided at a flow rate of from about 160 to about 240 SCCM.

56. The method of Claim 53, wherein the PECVD process is carried out at a power of from about 16 to about 24 watts, a pressure of from about 720 to 1080 mT and a temperature of from about 200 to 300 °C.